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A NEW LOOK AT THE ROLE OF CIRCUIT DESIGN ON ELECTRON DEVICE REL--ETC(U)
JAN 78 K A PULLEN

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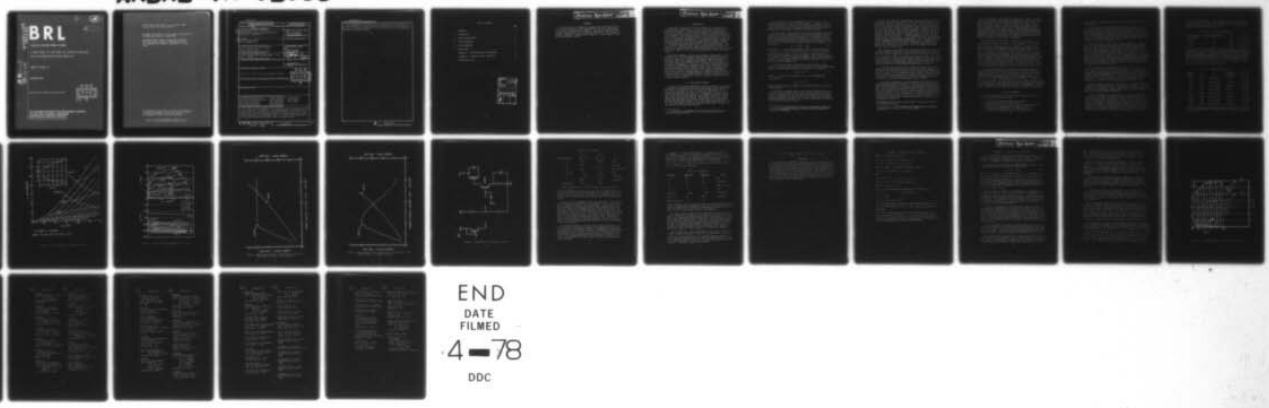

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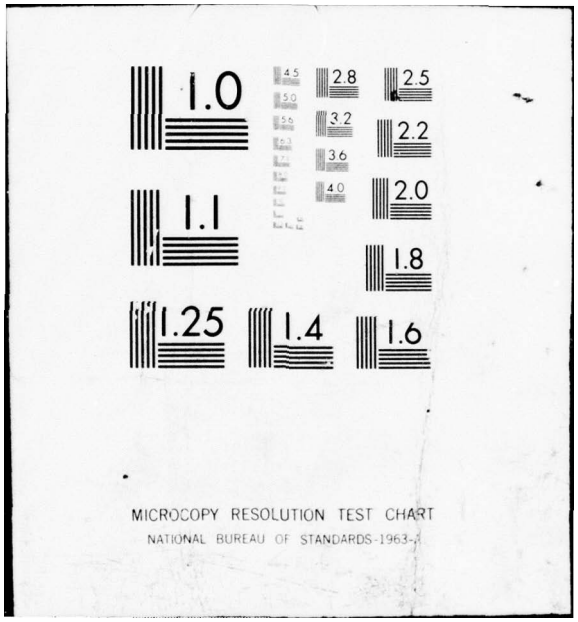
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TECHNICAL REPORT ARBRL-TR-02038

A NEW LOOK AT THE ROLE OF CIRCUIT DESIGN ON ELECTRON DEVICE RELIABILITY

Keats A. Pullen, Jr.

January 1978

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER (14) TECHNICAL REPORT ARBRL-TR-02038

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

(6) 4. TITLE *(and Subtitle)*
A NEW LOOK AT THE ROLE OF CIRCUIT DESIGN ON ELECTRON DEVICE RELIABILITY.

5. TYPE OF REPORT & PERIOD COVERED (9) Final rept.,

6. PERFORMING ORG. REPORT NUMBER

(10) 7. AUTHOR(s)
Keats A. Pullen, Jr.

8. CONTRACT OR GRANT NUMBER(s)

9. PERFORMING ORGANIZATION NAME AND ADDRESS
US Army Ballistic Research Laboratory
(ATTN: DRDAR-BLC-HN)
Aberdeen Proving Ground, MD 21005

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
(16) 1L662618AH80

11. CONTROLLING OFFICE NAME AND ADDRESS
US Army Armament Research & Development Command
US Army Ballistic Research Laboratory
(ATTN: DRDAR-BL)
Aberdeen Proving Ground, MD 21005

(11) 12. REPORT DATE
JAN [illegible] 1978 (12)

13. NUMBER OF PAGES
33 (27p.)

14. MONITORING AGENCY NAME & ADDRESS *(if different from Controlling Office)*

15. SECURITY CLASS. *(of this report)*
UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*
Approved for public release; distribution unlimited.

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17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

Transconductance Efficiency	Bipolar Transistor	Diffusion Mode
Screen-to-plate Transconductance	Plate Conductance	Miller Effect
Field-effect Transistor	Beta Limitations	Debye Region
Operational Reliability	Ebers-Moll Model	
Small-difference Problem	Power Limitation	

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The effect of circuit design on the reliability of both solid-state and tube-type active devices is considered. A new design approach is presented based on the Ebers-Moll model equations indicating that the proper use of device transconductance can lead to a substantial reduction in circuit voltage with at most a slight reduction in available power output. At the same time, considerably reduced power dissipation and improved device reliability result.

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Typical problems are examined which show improvements obtained compared to the usual approach to circuit design based on transistor beta characteristics. These detailed examples show the use and benefits of the new design approach as compared to traditional methods.

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FOREWORD

The author wishes to express his appreciation to the many individuals, both at BRL and at other organizations, for their contributions in the form of suggestions and comments. Among those from other organizations, he wishes to note in particular the efforts of Mr. Leonard Weisberg, ODDR&E; Mr. Bernard Reich, ECOM; Mr. G. Ross Kilgore, retired; and Mr. Ben Wolfe, retired.

I. INTRODUCTION

Operational reliability of circuits continues to be a problem of major importance, particularly in military electronic systems, but also in commercial systems. In recent years, emphasis has been placed on achieving increased reliability through fabrication of improved devices, yet the manner of use of the device in a circuit can have a substantially greater effect on the ultimate reliability of the combination. This factor is too frequently overlooked; it is assumed that circuit design problems have long been solved and that design rules are properly followed. Too frequently, circuit failure is blamed on device design or poor device specifications because the device is one of the most delicate links in the system. Although recent trends toward integrated circuits and large-scale integration have relieved the problem in some respects, because much of the circuit is built-in, this problem remains severe with power devices.

The natural tendency of the circuit designer in maximizing circuit performance is to use the maximum voltages consistent with device specifications. While on the surface this assumption appears reasonable, it typically ignores some fundamental and perhaps subtle limitations. In this paper, the basic factors involved in active circuit design are reexamined from fundamentals, leading to simple and straight-forward ways to assure that the inherent characteristics of solid-state devices and their associated circuits are properly used. Specific examples are provided for illustration of the use of the concepts and the benefits which can be derived. Although emphasis is placed on solid-state devices, electron tubes are also considered because of their continued importance in power circuits. Fortunately, the basic principles which must be applied are nearly identical.

II. BASIC DESIGN FACTORS

Present circuit design procedures for bipolar transistor application are generally focused around the current gain (beta), and stage voltage gain tends to be ignored.[1] This has several disadvantages. If in this design procedure, the supply voltage selected is too high, an incipient run-away condition can exist. Voltage gains in excess of about 10 to 20 per stage overall then may lead to phase instability, excess phase shift, or actual oscillation. Additionally, the circuit design depends (through beta) on a derivative with respect to a small difference between two large numbers, the collector and emitter currents. In any case, this approach leads to a condition where current runaway, and thus device failure, are both possible.

---

[1] R. D. Middlebrook, An Introduction to Junction Transistor Theory, John Wiley and Sons, 1957.

We consider here a different approach to optimizing the circuit in which the importance of beta is greatly reduced. In general, this design approach provides reduced circuit voltages and at most a slight loss in power output, but a considerably reduced power dissipation and improved circuit stability, and hence increased reliability.

All solid-state two-port amplifiers, including standard high-vacuum electron tubes can be represented in terms of the Ebers-Moll equations which are a special case of the equations for an admittance two-port. The Ebers-Moll equations provide a simple way to calculate the voltage gain, and in fact the appropriate equation for the simplest resulting circuit takes the form for the elementary amplifier (see Appendix A for derivation):

$$K_V = \kappa \Lambda I_c Z_L = g_m Z_L \qquad (1)$$

where kappa, κ, is the transconductance-per-unit-current efficiency, Λ is (q/kT), I_c is the collector current, and Z_L is the load impedance. With bipolar transistors, the value of kappa is approximately unity, and the value of lambda is 39 mhos per ampere. None of these parameters is a function of beta, and none of them depends sensitively on small differences of large numbers. The restriction on beta here is that it be above a specified minimum value.

It can be shown[2] that the approximate value of supply voltage required to achieve proper operation of an amplifier in the common emitter (source, cathode) mode of operation is defined by the equation:

$$|V_{cc}| \approx (\kappa)^{-1} \qquad (2)$$

where V_{cc} is the collector supply voltage. For the common base configurations:

$$|V_{cc}| \approx 7.5\ (\kappa)^{-1} \qquad (3)$$

These equations may also be applied to field-effect transistors and to electron tubes.

A key point to remember here is that the power handling ability of a bipolar transistor as an RF amplifier is basically and severely limited as a consequence of its high value for kappa, even in the common-base configuration. The effect of this basic limitation is frequently observed in practical circuits, but its cause is not always recognized. This point may be shown as follows:

---

[2] K. A. Pullen, The Enhancement of Electronics Reliability Through the Use of Transconductance Efficiency, AMSAA Technical Memorandum No. 123, 1972. AD 738535.

Consider the common-base configuration. Here the emitter-to-collector voltage gain may be as large as 75 to 100 for an overall gain of ten if the circuit is properly configured. For a peak collector current of 20 amperes, the forward (intrinsic) admittance may be as high as 750 mhos, for a maximum tuned impedance (loaded) of 0.1 ohm. Consequently, an output circuit may have to transform load impedances between 0.1 ohms and 50 ohms! The peak power input is 200 watts with a collector supply of ten volts (this assumes that 0.4 ohms may actually be used as an output impedance without instability -- somewhat doubtful at least), for an average of less than 100 watts. At 60 percent efficiency, one can expect at most fifty to sixty watts to be available.* This is observed in practice. Accordingly, the circuit should be designed in a manner potentially least destructive to the device rather than for achieving the maximum power theoretically possible. (The final stable power output differs little in either case!)

This limitation is not faced with tubes because of the very low values of kappa normally encountered. Supply voltages as high as 10 kv are often used, and the kappa values for devices used under these conditions will be between 10^{-3} and 10^{-4}, depending on the mode of use. For a peak plate current of 20 amperes again, the power input to such a tube can be as high as 200 kw, with an RF power output of approximately 50 kw. Field-effect transistors can potentially generate power to 1 kw per device if current capacity and voltage breakdown problems can be solved.

It should be realized that both electron tubes and FET devices have regions of operation under which their values of kappa do approach unity. With tubes, this mode of operation has been called "starved" operation. With FET devices, it is the operating region in which the potential jump across the Debye region provides the field controlling carrier flow in the channel. This diffusion mode can control the operation of FET devices for up to five orders of magnitude of drain current.[3]

In practical applications, all feedback paths that might affect the transconductance should be considered. One might think that the net effective transconductance is the prime factor limiting allowed voltage gain. This can be true if the principal feedback path is essentially at the external terminals of the device. Since it can be across the base-collector junction as well, it may be that the peak transconductance at the junction itself is the limiting factor. (With high-injection conditions in the NPN transistor, it may be at the external terminals as a consequence of the increase in transconductance due to minority-carrier concentration variations.)

*This applies unless internal stabilization is achieved with emitter stabilizing resistances.

[3] L. Evans and K. A. Pullen, Limitation of Properties of Field-Effect Transistors, Proc. IEEE, Vol. 54, p. 82, 1966.

We will now address some related design factors. First, if one does reduce the voltage, is there sufficient signal drive for the next stage? In reference to Equation 2, if kappa is approximately unity for a bipolar transistor, a supply voltage of only one volt greater than the device saturation voltage will satisfy typical requirements. With bipolar transistors, as with simple diodes, a 200 millivolt change in voltage applied across the input junction will cause over two thousand times change in device current. As long as the voltage from collector to emitter on a transistor exceeds the saturation voltage by even a few hundred millivolts, the transistor will amplify as well in most applications as it would with five or ten volts applied.

Second, normally in using higher voltages, a high value of Z_L is used to provide impedance matching. In this approach, Z_L must be lowered to keep the voltage gain down, or instability at least results. The limitation of the voltage gain per stage to approximately a given value, for example ten, requires limiting the effective value of Z_L. This is sometimes done intentionally, but frequently occurs accidentally. Examination of many typical commercial or military linear (including class C) amplifiers processing high-frequency signals shows quickly that there is usually one amplifier stage for each decade of voltage gain for RF and IF small-signal amplifiers. When design is based on beta and matched power gain (the usual procedure), it is necessary to use input loading from a following stage to reduce the voltage gain from as much as several hundred to a thousand down to the safe value of ten to twenty.

For a "super-beta" transistor inserted in a typically designed circuit, circuit oscillations can easily result, and can be incorrectly blamed on the transistor. The circuit should be designed with a lower-impedance output circuit having the proper "Q" value. Then, any transistor having a beta greater than five or ten probably would work as long as its f_α (alpha cutoff frequency) was high enough. In addition, the circuit would have the design amount of gain, because the stage would be designed to use a stabilized level of output current and the appropriate level of impedance, and its gain would not even be degraded by a nuclear event as long as the post-event beta exceeded a selected design minimum.

III. DESIGN PROCEDURE

The design procedure for discrete transistor amplifier circuits should be based on the following steps:

1. Selection of the desired output load impedance
2. Selection of the desired output current
3. Design of the bias circuit to provide selected output current
4. Selection of the appropriate base supply voltage
5. Selection of the appropriate collector supply voltage
6. Design of linear networks for use with the device

In some instances, steps one and two must be reversed in order or done simultaneously.

Reduction of heat dissipation through reduction of supply voltage for the output port of an active device reduces the amount of cooling required and can permit the sealing of the unit against dirt and moisture. Since input power is reduced, battery life for portable units can be increased substantially. Likewise, the ability to survive nuclear events can be increased, particularly if a small wire-wound decoupling resistor is used as a current limiting device for the active devices, which can look like short-circuits during an event.

If the "FET" resistor isn't used, two power supplies are required. This is not a disadvantage because of the reduced power requirements, and hence lower cost, of each power supply. The base supply, with typically ten volts available, is required to provide less than a tenth, often less than a twentieth, as much current as is required by the collector circuit, whereas the collector supply, providing most of the current, need supply only a tenth to a fifth as much voltage. As a result, the total net power required is from 10 to 25 percent of the usual total power. Good filtering is required, but little if any special regulation. Thus, the two power supplies need not cost more than the single supply, and the benefits from better circuit operation, less cooling required, and improved reliability are "free."

Both the input signal voltage required and the collector (drain, plate) supply voltage required for an active device are a function of the transconductance efficiency, as shown in Equation 2. Where maximum separation of signal from noise is required, use of devices with a maximum possible kappa is indicated, as this gives the maximum transconductance, and gain, for any level of current. (Noise level is largely current-dependent.) It should be noted, however, that space-charge effects help to minimize noise with both electron tubes and FET devices.

Where maximum power output is required, the use of devices with correspondingly reduced kappa values is indicated. In fact, one will find that with most high-power two-port electron tubes (triodes, tetrodes, pentodes), the recommended control supply voltage is within roughly a factor of two of that defined by Equation 2.

A key relationship in selecting tubes for a given circuit design is as follows. For tubes, the output current is strongly dependent on either the output supply voltage (the triode tube) or the voltage on an auxiliary power-control electrode (the screen grid for tetrodes and pentodes). Accordingly, the power-handling capability for the tube is determined by the rate of change of output current with either output voltage or the auxiliary electrode voltage. The amplification factor should not be the prime consideration for tube choice, but instead the ability to pass current as measured by g_m and g_p must be considered.

The importance of this is shown in Tables I and II for triodes and pentodes. Three triodes are listed in Table I, all of them having the same amplification factor and about the same power dissipation although greatly different output power capabilities:

Table I. Triode Power Capabilities

Tube Type Number	Amplification Factor	g_m	g_p
6C4, 12AU7	20	2500	177 micromhos
12BH7	20	8000	340 micromhos
5687	20	12500	613 micromhos

The values given are tabulated at zero grid bias and half of peak power dissipation. Table II is a similar table for pentodes, but it shows the range of characteristics for several useful tubes. Whereas the important parameter defining power-handling ability for triodes is plate conductance, for tetrodes and pentodes it is screen-to-plate transconductance, g_{m2}. The g_m and g_{m1} in these tables are the transconductances from the control grid to plate for the respective tubes. The values of Z_L are calculated for the desired output voltage.

Table II. Pentode Power Capabilities

Tube Type Number	g_{m1}	g_{m2}	Ideal Screen Voltage	Typical Z_L (100 V out)
6BH6	5000	110 micromhos	95 volts	8000 ohms
6AK5	7000	220 micromhos	95 volts	7000 ohms
5686	3750	420 micromhos	130 volts	3300 ohms
6CL6	12500	504 micromhos	110 volts	2500 ohms
6216	14000	1620 micromhos	80 volts	1330 ohms
6BQ6T	11000	1980 micromhos	65 volts	1250 ohms
6DQ6A	9000	3470 micromhos	70 volts	800 ohms
6DQ5	16000	5400 micromhos	60 volts	420 ohms

Clearly, the lower the required load impedance which must be accepted for a given voltage output, the farther down this table one should make his selection.

In addition, a set of typical triode and a set of pentode curves designed to make optimum use of transconductance-type data are shown in Figures 1 and 2.[4,5] These curves have been information engineered, as have the corresponding transistor curves, to maximize ease of use of the data in effective design, Figure 3.[6]

It is noteworthy that Z_L determines the frequency limit in circuits such as the vertical deflection circuit for an oscilloscope. While tubes such as the 6CL6 have been used extensively in this application, it can be seen from Table II that this may not be the optimum choice.

With typical circuits, the output capability of the circuit varies with the value of the appropriate power-control voltage as shown in Figure 4 for ordinary amplifiers. As can be seen, the output power available rises to a certain value, then levels, whereas the input power continues to increase. (The difference in power scales should be noted.) With frequency multipliers based on electron tubes, the output capability can vary as shown in Figure 5 as a consequence of the fact that the conduction angle in the active device may increase rapidly with an increase of the power-control voltage. At the peak power point, the conduction angle at the output frequency is 180 degrees. In all cases, the power input increases at least linearly with the increase of power-control voltage. With electron tubes, it usually increases at the 2.6 exponent with respect to the control voltage. Clearly, optimum power efficiency occurs near a supply voltage defined by $(\kappa)^{-1}$.

IV. DESIGN EXAMPLES

Example I. A 10.7 MHz IF Amplifier - overall stage gain of ten. Design both by the standard technique (matched impedances) and using the transconductance technique. The circuit configuration is shown in Figure 6, and typical device curves in Figure 3.

Take: I_c = 1.0 ma.
f = 10.7 MHz
V_{cc} = 1 volt, 10 volts
V_{bb} = 10 volts

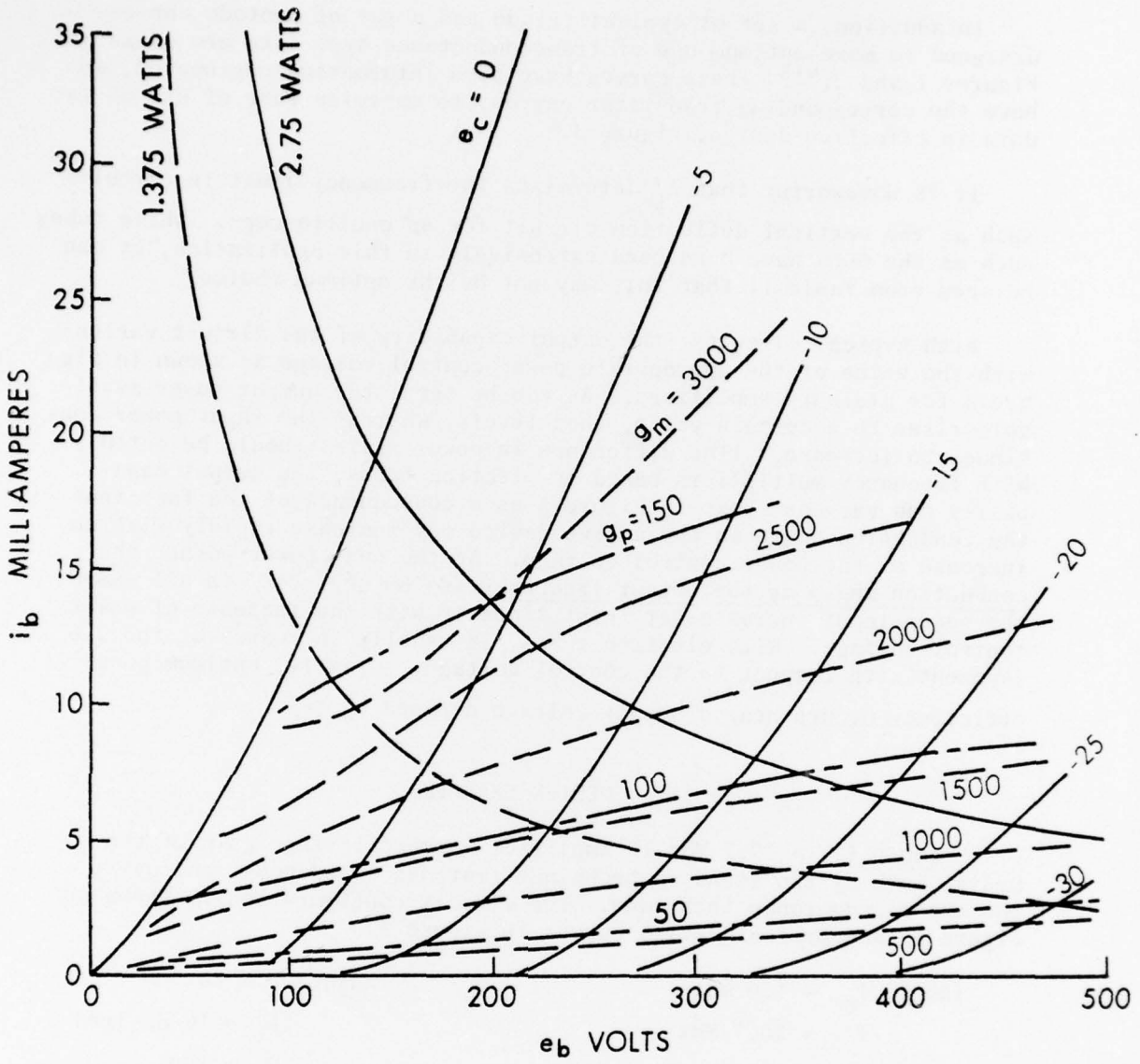
Assume $\beta > 20$
K_V = 10 desired
Q_L = 100

---

[4] K. A. Pullen, Conductance Curve Design Manual, John F. Rider Publisher, Inc., 1959.

[5] K. A. Pullen, Conductance Design of Active Circuits, John F. Rider Publisher, Inc., 1959.

[6] K. A. Pullen, Reliable Military Electronics, AMCP 706-124, 1976. May be obtained from DDC or NTIS. This is an update of K. A. Pullen, Handbook of Transistor Circuit Design, Prentice-Hall, Inc., 1962.



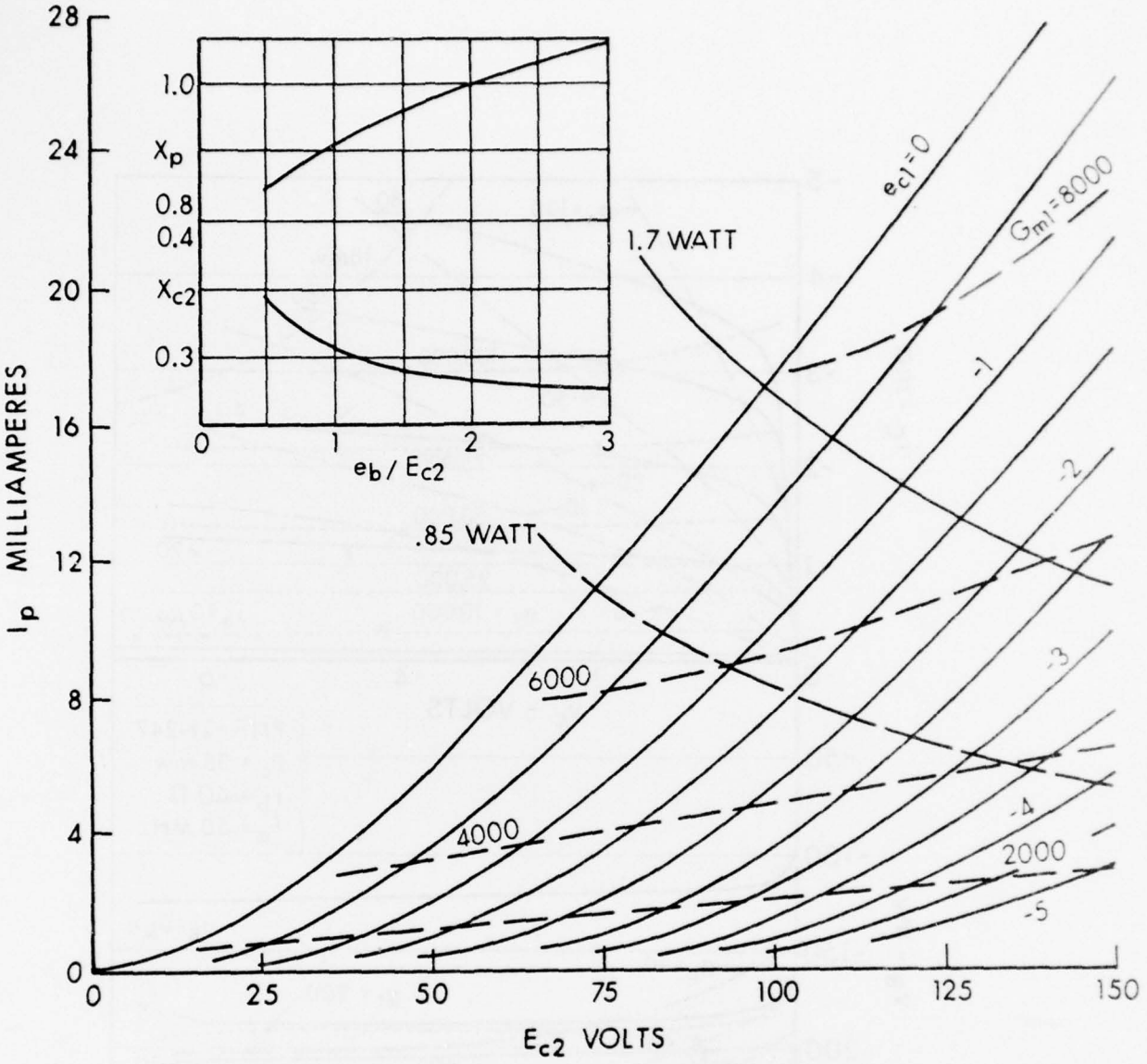
6135: P_p 3.5 WATTS

BASE: 1 5-P 2-1C 3 4-H 6-G 7-K

5814A: P_p 2.75 WATTS

BASE: 1-P_2 2-G_2 3-K_2 4 5-H 6-P_1 7-G_1 8-K_1 9-HCT

Figure 1. Typical Triode Tube Augmented Curves, 12AU7/5814A



P 1.7 WATT: P 0.5 WATT

BASE: 1-G_1 2-K 3 4-F 5-P 6-G_2 7-K-G_3

Figure 2. Typical Pentode Tube Augmented Curves, 6AK5

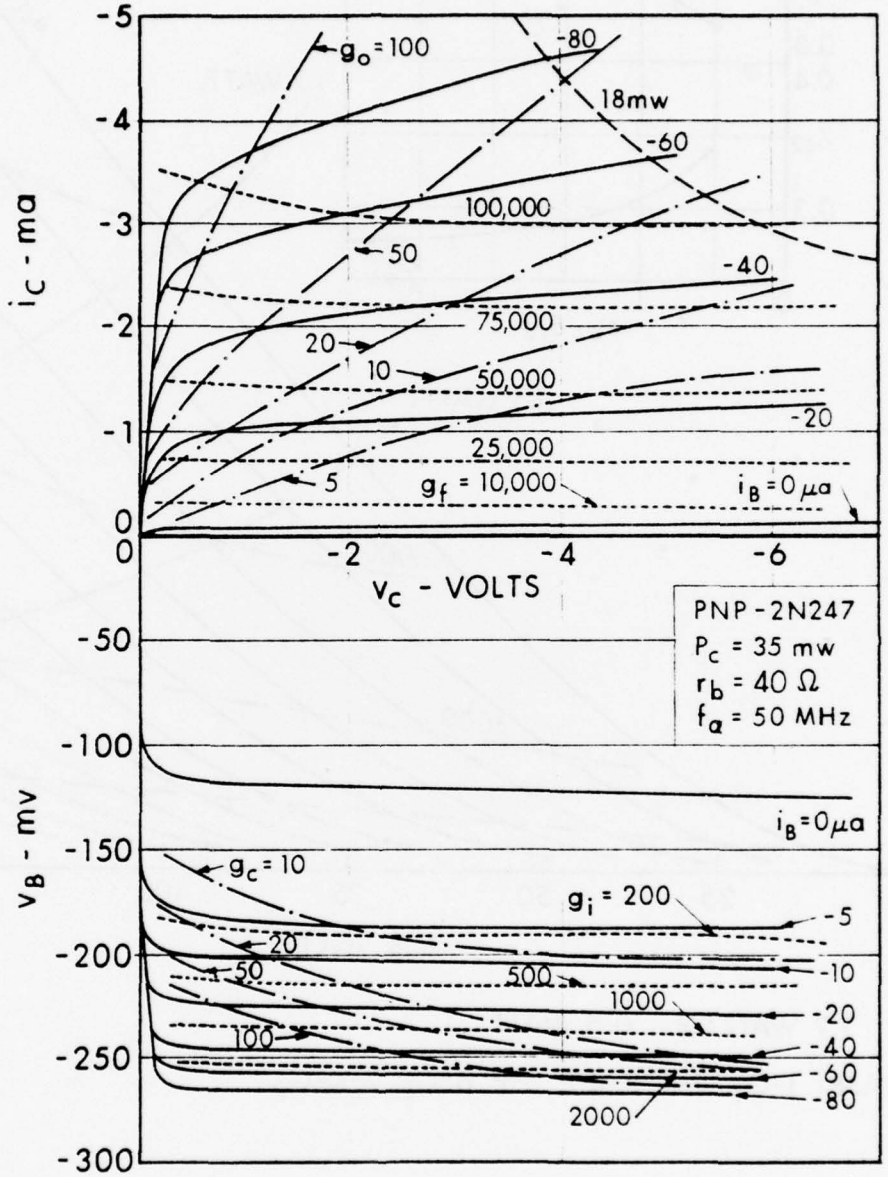


Figure 3. Typical Transistor Augmented Curves, 2N247

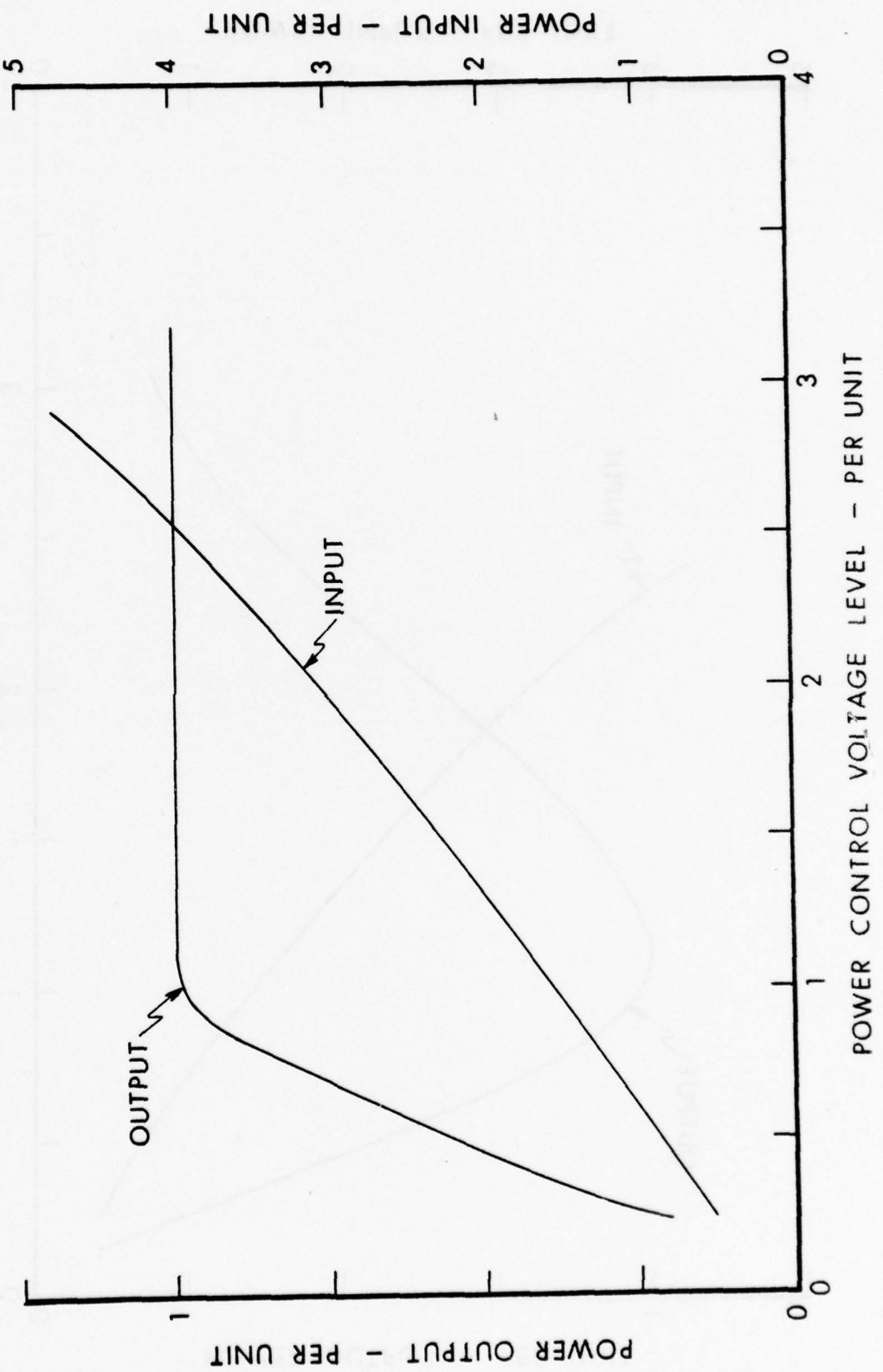


Figure 4. Sample Power Input and Output Curves as a Function of Power Control Voltage -- Linear Amplifier

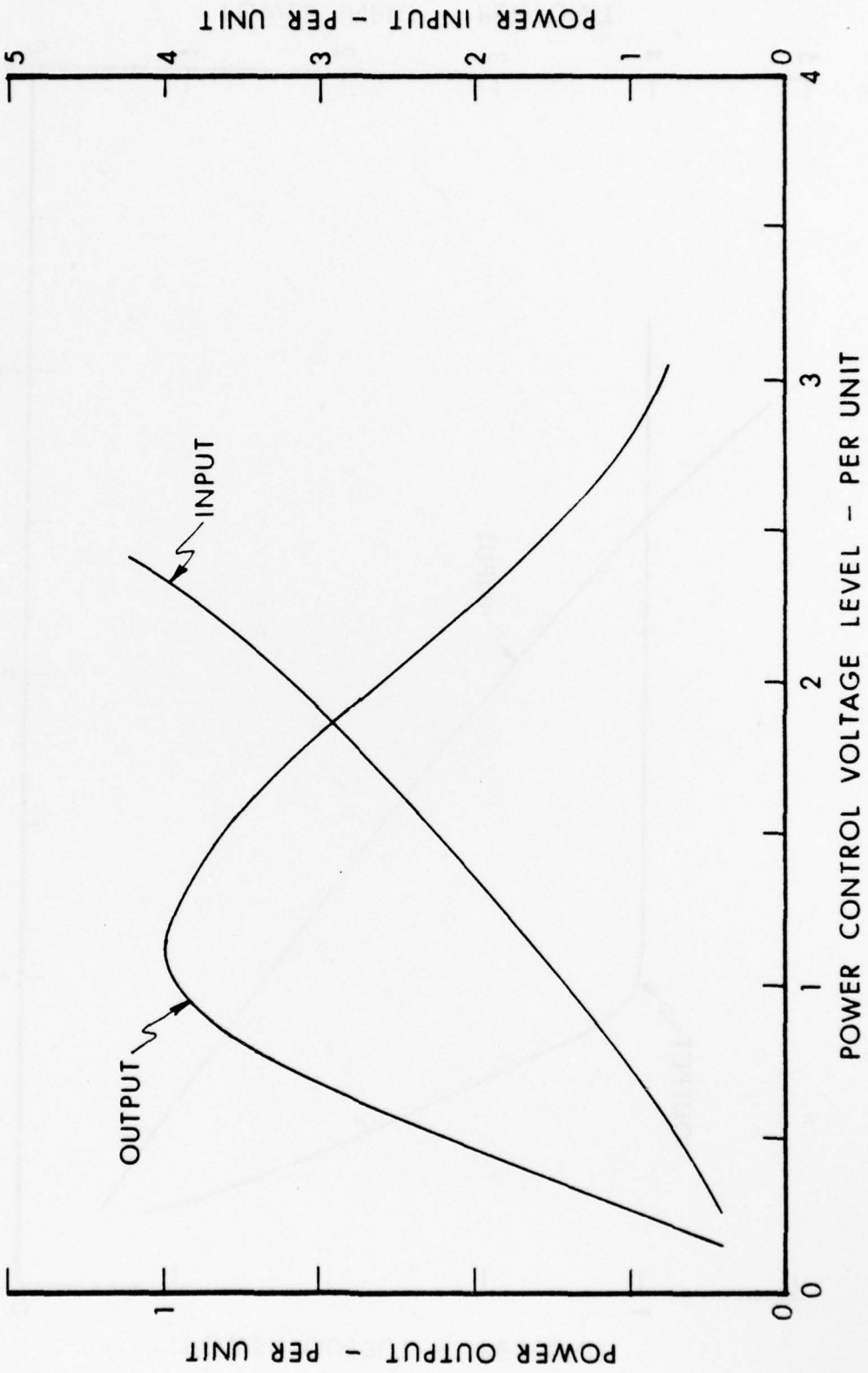


Figure 5. Sample Power Input and Output Curves as a Function of Power Control Voltage -- Frequency Multiplier

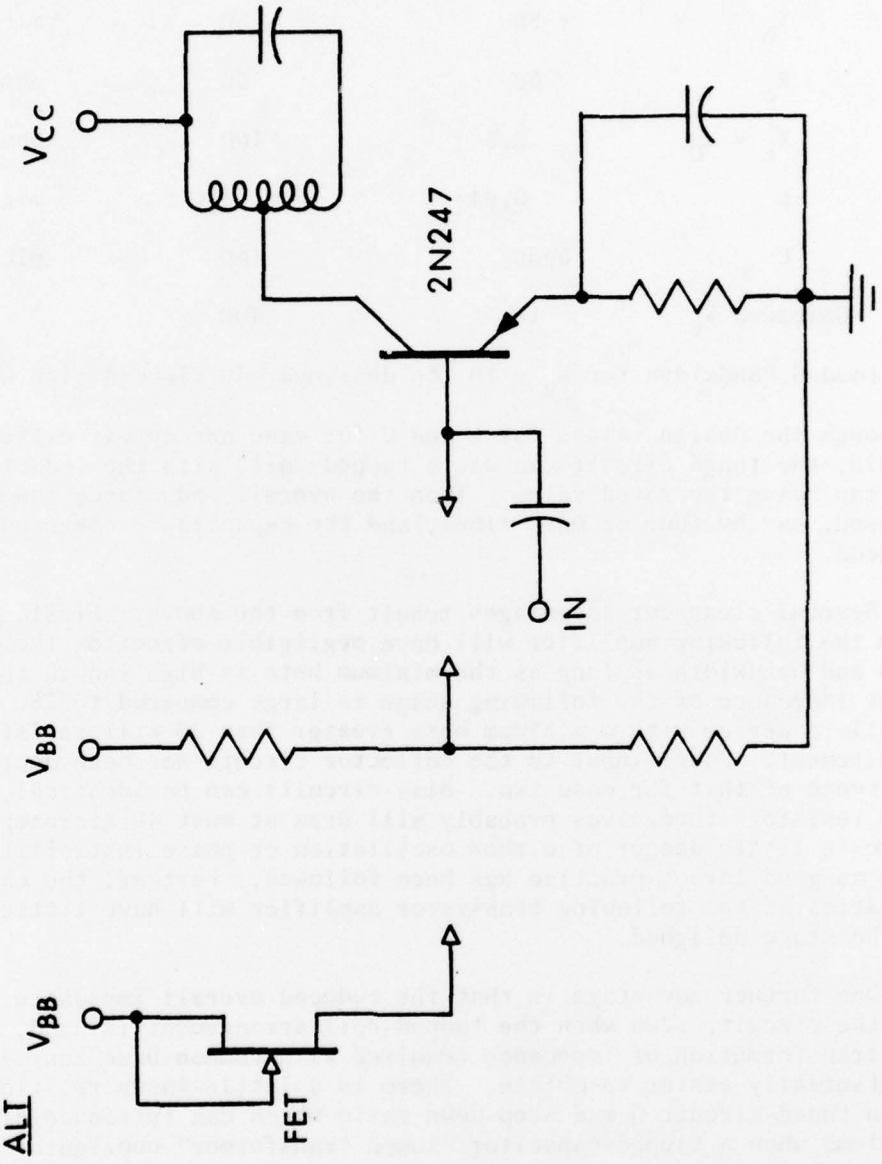


Figure 6. Typical Basic IF/RF Amplifier Circuit

Table III. Design Data

Parameter Results	Case 1 (V_{cc} = 1 v)	Case 2 (V_{cc} = 10 v)	Units
Z_L	250	10000	ohms
I_b	< 50	< 50	micromhos
R_e	50	50	ohms (bypassed)
$X_L = X_C$	2.5	100	ohms
L	0.04	1.6	microhenry
C	6400	160	picofarads
Unloaded K_v	10	400	

Loaded bandwidth for K_v = 10 As designed 40 times design width

Although the design values for L and C for case one appear difficult to obtain, the tuned circuit can use a tapped coil, with the inductance to the tap being the rated value. Then the overall inductance can be increased, say by four or more times, and the capacitance correspondingly reduced.

Several clear-cut advantages result from the above. First, loading from the following amplifier will have negligible effect on the stage gain and bandwidth as long as the minimum beta is high enough that the input impedance of the following stage is large compared to 250 ohms. Usually a device with a minimum beta greater than 20 will satisfy the requirement. Power input to the collector circuit has been decreased to one-tenth of that for case two. Bias circuits can be identical, and the bias resistors themselves probably will draw at most 40 microamperes. There is little danger of either oscillation or phase instability as long as good layout practice has been followed. Further, the characteristics of the following transistor amplifier will have little effect on the stage designed.

One further advantage is that the reduced overall impedance level for the circuit, even when the tapped-coil arrangement is used, makes the transformation of impedance required with common-base configurations substantially easier to obtain. There is a little-known relation between tuned-circuit Q and step-down ratio which can introduce circuit problems when a tapped-capacitor "tuned transformer" configuration is used. This problem can be significantly alleviated with the proposed design procedure.

Example 11. Design a power amplifier - to operate at 25 MHz. In this instance, the goal is to build up the power level of an RF source. The prime option therefore is obtaining power gain, to a lesser extent, voltage gain. Assume a two-stage design; let the voltage gain for each stage be two, with the input signal starting at 10 millivolts. Take I_{c1} as 1 ma; I_{c2} as 5 ma. Choose the Q value for the loaded tuned circuits to be 25. Take V_{cc} to be one volt:

Table IV. Design Data

Parameter	Stage One	Stage Two	Units
Z_L	50	10	ohms
I_b	< 50	< 200	microamperes
R_e	50	10	ohms (bypassed)
$X_L = X_C$	2	0.4	ohms
Effective L	0.032	0.006	microhenries
Effective C	640	3200	picofarads
Minimum stage beta	25	25	

Clearly, tapped coils or transmission lines are required, and the difficulty of designing adequate parallel-tuned circuits for very-high-frequency transistor amplifiers is also strongly demonstrated. Where it is possible, the use of series-tuned circuits is recommended.

The output signal voltage with this amplifier will be 40 millivolts, and the variation in voltage gain of an amplifier following the second stage with instantaneous signal voltage will be about four to one. (The third stage would approach class C operation.) But the signal-frequency current available from stage two in this semi-power amplifier arrangement may be as much as two milliamperes rms, or possibly a little more. As long as the minimum required beta is available for the respective transistors, stable operation in the designed mode can be achieved. A further RF design, of a class C amplifier, is detailed in Appendix B.

Other Applications: Since transconductance as a function of device current is readily available in terms of I_c in Equation 1, calculation of properties of nonlinear circuits, including frequency multipliers, mixers, and switching circuits, is relatively straight-forward. Conversion conductance, which is important with both mixers and frequency multipliers, is defined in terms of the equation:

$$g_c = 0.25\ (g_{mmax} - g_{mmin}) \approx 0.25\ (I_{cmax} - I_{cmin}) \qquad (4)$$

V. CONCLUSIONS

Some of the most important consequences of the described approach for the design of transistor circuits, in addition to its unique benefit in achievement of reliability, are first that it leads to an academically simple and straight-forward way of analyzing the characteristics of solid-state devices and their associated circuits, and second the fact that dependence on a derivative with respect to a small difference between collector and emitter currents is greatly reduced. First-cut estimation of a circuit's behavior is both simplified and made more exact, and a better means for optimizing the circuit is available because of the reduced importance of the beta parameter.

APPENDIX A - DERIVATION OF BASIC EQUATIONS

Simplified Ebers-Moll Equations:

$$i_b = I_{b0} + I_{b1} \exp \Lambda v_b + I_{b2} F_b (v_b, v_c)$$

$$i_c = I_{c0} + I_{c1} \exp \Lambda v_b + I_{c2} F_c (v_b, v_c)$$

where $\Lambda = (q/kT) = 39 \text{ (volts)}^{-1}$ (or mhos per ampere)

$$(\partial i_c / \partial v_b) = \Lambda I_{c1} \exp \Lambda v_b + I_{v2} (\partial F_c / \partial v_b)$$

But

$$I_{c1} \exp \Lambda v_b = i_c - I_{c0} - I_{c2} F_c (v_b, v_c) = \kappa i_c$$

$$(\partial i_c / \partial v_b) = \kappa \Lambda i_c + I_{c2} (\partial F_c / \partial v_b) = g_m \approx \kappa \Lambda i_c$$

But $K_v = - g_m Z_L = \kappa \Lambda i_c Z_L$

Since $i_c Z_L$ has dimensions of voltage, and is related to V_{cc},

$$i_c Z_L = \eta V_{cc} \qquad (0.3 \leq \eta \leq 1.0)$$

$$K_v = - \eta \kappa \Lambda |V_{cc}|$$

or $|V_{cc}| = |K_v| / \eta \kappa \Lambda \approx (\kappa)^{-1}$

For bipolar transistors, kappa has a value approximating unity, with limits of approximately 0.6 to 1.5. Both I_{c0} and I_{c2} are normally negligible.

For FET devices and electron tubes, the difference between I_{c0} and i_c may be substantially less than i_c. This gives a range for kappa for these devices of from 10^{-5} to 10^{-2}. Under specialized conditions the value may approach unity with both kinds of devices.

APPENDIX B - DESIGN OF CLASS C AMPLIFIER

Since common practice with transistorized RF power amplifiers in the past has been to use a collector supply voltage as high as second-breakdown and fundamental breakdown for a device permits, the following analysis is designed to evaluate the validity of this practice.

Any amplifier is to some extent a feedback amplifier, and its operating equation therefore takes the simplified form:

$$K = K_V/(1 - K_f K_V) \qquad (II-1)$$

where K is the overall voltage amplification, K_V is the forward voltage amplification, and K_f is the amplification (much less than unity) for the feedback path of the amplifier. As long as the overall value of K as a function of frequency does not include a zero value for the denominator, the circuit should be stable, but if minimum-phase characteristics are also required, the magnitude of $K_f K_V$ should be as small as possible with respect to unity.

Because of the assortment of stray inductances and capacitances in RF amplifier circuits, it must be assumed that if the magnitude of $K_f K_V$ can approach unity, unstable conditions can occur, and the phase transfer function of the amplifier will be excessively erratic as a function of frequency. As a matter of fact, the existance of excess phase shift is probably the most sensitive indicator of a potentially unstable amplifier, one which might "self-destruct."

Efficiency considerations require that power stages be operated in the common-base configuration, as otherwise the ratio of peak available energy taken from the tuned circuit to loss in the active device may be as small as two, whereas in the common-base (C-B) configuration it may be more than ten. The point of conversion from use of the common-emitter (C-E) configuration to the C-B configuration is this one of the critical points in design of power amplifier circuits -- getting adequate drive for the first C-B amplifier and assuring phase stability at the same time can be difficult.

As has been noted, with proper design and layout, it is possible to get stable operation in the C-E mode with input-to-output voltage gains of up to ten, and in the C-B mode with gains of approximately 100 (emitter to collector). This means that the maximum feedback "gain" in the two cases typically cannot be allowed to exceed either 0.01 or 0.001.

The feedback paths for transistors at high frequencies are principally capacitances, and, particularly in the C-E mode, these may be substantial. There are both intrinsic capacitances, those inherent in the junction themselves, and parasitic, those due to case and wiring. Any of

these capacitances can prove to be critical in any given application. They are particularly severe in the C-E mode, since there is no effective isolation between input and output, and neutralization or unilateralization is difficult to achieve because of the complexity of the equivalent circuit in this configuration.

With existing values of feedback capacitances, the only available approaches to limiting K_f are really three, namely, resonating the capacitance in a parallel mode to reduce coupling, neutralization, and reduction of input and output effective impedance levels. Of the three, the reduction of the effective impedance level is often the only viable approach where phase stability and absence of potential parasitics are important.

Theory shows that for maximum effective bandwidth for a chain of amplifiers using discrete circuit elements in the presence of Miller capacitance, stage voltage gains between two and three are optimum. In practice, other considerations may apply, with the result that voltage gains typically should not exceed ten to twenty overall (input to input) at the most.

For efficient operation of a transistor in a class C amplifier, it is essential that the collector-to-emitter voltage be as small as possible during the current pulse which "charges" the frequency-determining components of the circuit. The supply voltage then must be sufficient to produce this voltage at peak current with the allowed value of loaded tuned impedance.

When the operating load line for these conditions is established for a class C amplifier, it appears that somewhat as sketched at "D" in Figure B-1. The dotted section develops as a result of energy exchange in the frequency stabilizing circuit. The actual load contour starts initially through the V_{cc} point and within "Q" cycles has essentially moved to the indicated location. (Strictly, an elliptic load contour is generated, leading to energy storage which is vital in circuit operation.) The shift in load-line position is accounted for in the equation for V_{cc} in Appendix I by the eta factor, which may have a value as small as 0.3.

The direction of traversal of the elliptic load contour is indicated by the arrowheads on the graph. As the coupling to the load is tightened, the resistive axis of the load line shifts as from A to D for a properly selected value of V_{cc}, and as from A' to D' for an excess voltage situation.

When the transistor amplifier is being operated near its f_{max}, it may be necessary to increase the selected value of V_{cc} sufficiently to assure that the load contour is properly located with respect to existing f_{max} contours. This condition in fact may indicate that the device chosen is

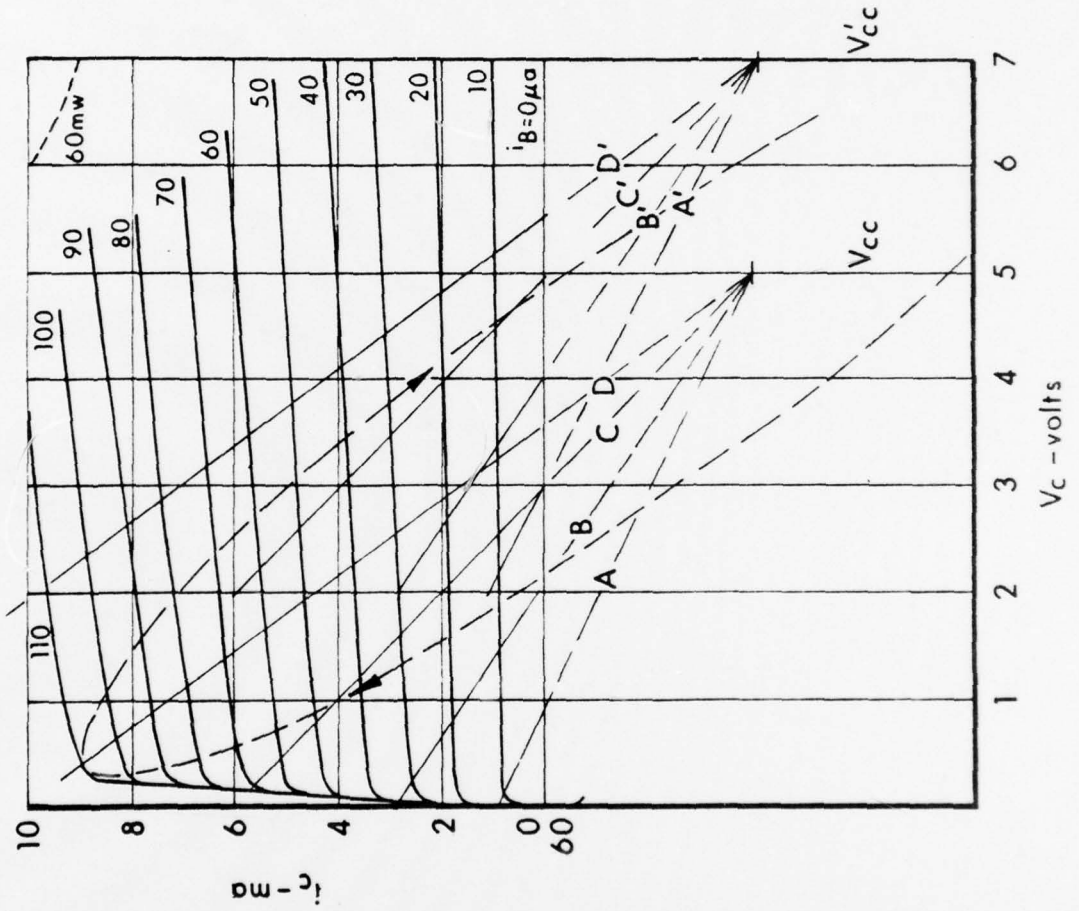


Figure B-1. Operating Contours -- Sample Class C Amplifier

not suitable for the intended application. Where possible, such a voltage boost should be avoided.

The important point to note from the attached plot is that with "matched impedances," the voltage gain in the power amplifier (as shown by C") quickly develops a maximum value so great that stability can no longer be assured. As the impedance is reduced through loading to assure stability, the transistor power input increases and at the same time the power output at the chosen output frequency may decrease. The only way this situation may be avoided is by the selection of a reduced value of collector supply voltage.

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